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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,414	08/05/2003	Mark J. Kuzawinski	END920020102US1	7945

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Jack P. Friedman
Schmeiser, Olsen & Watts LLP
Suite 201
3 Lear Jet Lane
Latham, NY 12110

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,414	KUZAWINSKI ET AL	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *23 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 10-22* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/5/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/634414 Attorney's Docket #: END920020102US1
Filing Date: 8/5/2003;

Applicant: Kuzawinski et al.

Examiner: Alexander Williams

Applicant's election with traverse of species of figures 3A, 3B and 4 (claims 1-22), filed 10/20/2003, has been acknowledged.

This application contains claims 23 and 24 drawn to an invention non-elected with traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim 21 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation "The method of claim 1" in claim 21. There is insufficient antecedent basis for this limitation in the claim.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-4 and 10-22, **insofar as claim 21 can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Yeh et al. (U.S. Patent # 6,489,682 B1).

1. Yeh et al. (figures 1 to 8) specifically figures 7 and 8 show an integrated circuit package **400** for holding an integrated circuit die **401** and connecting a set of circuit bond pads **406** on the die to a set of package bond pads **404** disposed on a first surface of the package, the package bond pads being arranged in a set of package bond pad modules such that at least one pair of individual package bond pads is disposed with a

package bond pad module overlap in an overlap area along a transverse axis extending substantially perpendicular to the die, a first package bond pad of said pair being connected to a first via **403v** positioned inward of said overlap area and a second package bond pad of said pair being connected to a second via **405v** positioned outward of said overlap area, all of said first package bond pad, said first via, said second package bond pad and said second via being disposed within one of said package bond pad modules and forming a via sub-module, each of said package bond pad modules having a package module pitch along a longitudinal axis parallel to a side of said integrated circuit die.

US-PAT-NO: 6489682
DOCUMENT-IDENTIFIER: US 6489682 B1
TITLE: Ball grid array semiconductor package and substrate therefor
DATE-ISSUED: December 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yeh; Yung I	Kaohsiung	N/A	N/A	TW
Ma; Shu Jung	Kaohsiung	N/A	N/A	TW
Hsien; Shiun Jaw	Kaohsiung	N/A	N/A	TW

(6) FIGS. 1 and 2 depicts a conventional BGA semiconductor chip package 100 with a chip 101 mounted on a substrate 102 which has a ground ring 103, two power rings 104 and a plurality of fingers 105. A number of bonding pads 106 are connected to the ground ring 103, two power rings 104 and a plurality of fingers 105 by bonding wires 107a-107d respectively. An area array of solder balls 108 are disposed at the lower surface of the substrate 102 for electrically connecting to the ground ring 103, the power ring 104, the fingers 105, the ground plate 103g and the power plate 104p through the vias 103v, 104v and 105v respectively. Each solder ball 108 is used for electrical connection to external circuit, such as a printed circuit board. Finally, a package body (not shown) encapsulates the chip 101, bonding wires 103 and the substrate 102 to form a BGA semiconductor package structure.

(6) Referring to the FIGS. 3 and 4, they illustrate another conventional BGA semiconductor package structure 200 which includes a chip 201 mounted on a substrate 202 on which there are two ground rings 203 and 203', two power rings 204 and 204' and a plurality of fingers 205. The bonding pads 206 on the chip 201 surface are connected to the two ground rings 203 and 203', the two power rings 204 and 204' and the fingers 205 through bonding wires 207a-e. An area array of solder balls 208, attached to the lower surface of the substrate 202, are electrically connected to the ground rings 203 and 203', the power rings 204 and 204' and the fingers 205 on the upper surface of the substrate through the vias. Last, a package body (not shown) encapsulates the chip 201, bonding wires 207 and the upper surface of the substrate to form a BGA semiconductor package structure 200. In this BGA semiconductor package structure, the bonding wire with five different looping profiles 207a-e are required for electrically connecting the bonding pads 206 to the ground rings 203 and 203', the power rings 204 and 204' and the fingers 205.

(7) FIGS. 7 and 8 show the second preferred embodiment of the BGA semiconductor package 400. The BGA semiconductor package 400 includes a chip 401 mounted on a substrate 402 which compromises an upper surface 402a, a lower surface 402b, a ground plate 403g positioned under the upper surface 402, at least one power plate 404p between the ground plate 403g and the lower surface 402b. The upper surface 402a possesses two ground rings 403 and 403', two power rings 404 and 404', and a plurality of fingers 405. The bonding pads 406 on the chip 401 surface are connected to the two ground rings 403 and 403', the two power rings 404 and 404' and the fingers 405 through bonding wires 407a, 407b and 407c, respectively. An area array of solder balls 408, attached to the lower surface of the substrate 402, are electrically connected to the two ground rings 403 and 403', the two power rings 404 and 404' and the fingers 405 on the upper surface of the substrate 402, and to the ground plate 403g and power plate 404g through the vias 403v, 404v, 405v. Last, a package body (not shown) encapsulates the chip 401, bonding wires 407a, 407b, 407c, and the upper surface 402a of the substrate 402 to form a BGA semiconductor package structure 400.

2. A package according to claim 1, Yeh et al. show in which each package bond pad module contains a subset of bond pads equal in number to a corresponding number of circuit bond pads disposed in said die within said package module pitch.

3. A package according to claim 1, Yeh et al. show in which at least one connection for DC power passes through a via sub-module located along said transverse axis at a first position.
4. A package according to claim 3, Yeh et al. show in which at least two connections for DC power pass through corresponding first and second via sub-modules located at said first position along said transverse axis and in separate package bond pad modules.
10. Yeh et al. (figures 1 to 8) specifically figures 7 and 8 show an integrated circuit package **400** for holding an integrated circuit die **401** and connecting a set of circuit bond pads **406** on the die to a set of package bond pads **403** disposed on a first surface of the package, the package bond pads being arranged in a set of package bond pad modules such that at least two pairs of individual package bond pads are disposed having a package bond pad module overlap in at least two overlap areas along a transverse axis extending substantially perpendicular to the die, a first package bond pad of each of said pairs being connected to a first via **403v** positioned inward of said overlap area and a second package bond pad of each of said pairs being connected to a second via **405v** positioned outward of said overlap area, all of said pairs of package bond pads and associated vias being disposed within one of said package bond pad modules and forming a via sub-module, each of said package bond pad modules having a package module pitch along a longitudinal axis parallel to a side of said integrated circuit die.
11. A package according to claim 10, Yeh et al. show in which each package bond pad module contains a subset of bond pads equal in number to a corresponding number of circuit bond pads disposed in said die within said package module pitch.
12. A package according to claim 10, Yeh et al. show in which at least one connection for DC power passes through a via sub-module located along said transverse axis at a first position.
13. A package according to claim 12, Yeh et al. show in which at least two connections for DC power pass through corresponding first and second via sub-modules located at said first position along said transverse axis and in separate package bond pad modules.
14. A package according to claim 10, Yeh et al. show in which no connection for DC power passes along a conductive member that passes substantially parallel to a longitudinal axis substantially perpendicular to said transverse axis through substantially all of a subset of package bond pad modules on an edge of said die.

15. A package according to claim 14, Yeh et al. show in which each package bond pad module contains a subset of bond pads equal in number to a corresponding number of circuit bond pads disposed in said die within said package module pitch.
16. A package according to claim 10, Yeh et al. show in which at least one connection for DC power passes through a via sub-module located along said transverse axis at a first position.
17. A package according to claim 10, Yeh et al. show in which at least two connections for DC power pass through a single via sub-module located at a first position along said transverse axis.
18. Yeh et al. (figures 1 to 8) specifically figures 7 and 8 show a method of forming an integrated circuit package **400** for holding an integrated circuit die **401** and connecting a set of circuit bond pads **406** on the die to a set of package bond pads **403** disposed on a first surface of the package, the package bond pads being arranged in a set of package bond pad modules such that at least one pair of individual package bond pads is disposed in a package bond pad module overlap in an overlap area along a transverse axis extending substantially perpendicular to the die comprising the steps of forming an insulating substrate **402** including a set of vias **403v,405v** extending from a top surface to a set of lower interconnection members; forming said set of bond pad modules, including forming said pair of individual package bond pads with a first package bond pad of said pair being connected to a first via positioned inward of said overlap area and a second package bond pad of said pair being connected to a second via positioned outward of said overlap area, all of said first package bond pad, said first via, said second package bond pad and said second via being disposed within one of said package bond pad modules and forming a via sub-module, such that each of said package bond pad modules has a package module pitch along a longitudinal axis parallel to a side of said integrated circuit die.
19. A package according to claim 18, Yeh et al. further comprising a step of forming at least one connection for DC power passing through a via sub-module located along said transverse axis at a first position.
20. A package according to claim 18, Yeh et al. further comprising a step of forming at least two connections for DC power passing through corresponding first and second via sub-modules located at said first position along said transverse axis and in separate package bond pad modules.

21. The method of claim 1, Yeh et al. show wherein no edge of the first package bond pad is not aligned with any edge of the first via.
22. The method of claim 21, Yeh et al. show wherein no edge of the second package bond pad is not aligned with any edge of the second via.

Claims 5 to 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Any such indication as to the allowability of these claims is reserved until which time a suitable response is filed.

The following listed are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,691,698,696,784,786,774,680,773,692,693,778,782 361/794,777,780	1/9/05
Other Documentation: foreign patents and literature in 257/700,701,758,691,698,696,784,786,774,680,773,692,693,778,782 361/794,777,780	1/9/05
Electronic data base(s): U.S. Patents EAST	1/9/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/10/05